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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/891,325	06/27/2001	Osamu Samuel Nakagawa	10005208-1	3642

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HEWLETT-PACKARD COMPANY
Intellectual Property Administration
P.O. Box 272400
Fort Collins, CO 80527-2400

EXAMINER	
LUU, CHUONG A	
ART UNIT	PAPER NUMBER
2818	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	12/28/2006	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	09/891,325	NAKAGAWA, OSAMU SAMUEL	
	Examiner	Art Unit	
	Chuong A. Luu	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12/07/2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

Applicant's arguments with respect to claims 1-12 have been considered but are moot in view of the new ground(s) of rejection.

PRIOR ART REJECTIONS

Statutory Basis

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

The Rejections

Claims 1-9 and 12 are rejected under 35 U.S.C. 102(e) as being anticipated by Hirano et al. (U.S. 6,163,043).

Hirano discloses a semiconductor device with

(1) a first electrode (111a) formed during a first deposition of a first metal layer (111a) of a multi-level semiconductor device;

a first dielectric layer (113) configured to be deposited over said first electrode (111a);

a second electrode (112a) formed during a second deposition of a second metal layer (112a) of said multi-level deposition device, wherein said second electrode (112a) is deposited on an interface of said first dielectric layer (113), wherein said on-chip capacitor is formed in a crossover area of said first metal layer (111a) and said second metal layer (112a) of said multi-level semiconductor device;

a second dielectric layer (104) also deposited on the interface of said first dielectric layer (113) (see Figure 2);

(2) wherein an angle of intersection between said first metal layer (111a) and said second metal layer (112a) is between zero and ninety degrees (see Figure 2);

(3) wherein said first electrode (111a) and said second electrode (112a) are configured to be substantially parallel (see Figure 2);

(4) wherein said first electrode (111a) and said second electrode (112a) are further configured to be overlapping (see Figure 2)

(5) wherein said first electrode (111a) and said second electrode (112a) are configured as a rectangular planar structure (see Figure 2);

(6) wherein said first electrode (111a) and said second electrode (112a) are substantially parallel and overlapping (see Figure 2);

(7) wherein said substantially thin dielectric material comprises a composite of materials (see Figure 2);

(8) a first electrode (111a) formed during a first deposition of a first metal layer (111a) of a multi-level semiconductor device;

a substantially thin dielectric layer (113) configured to be deposited over said first electrode (111a);

a second electrode (112a) formed during a second deposition of a second metal layer (112a) of said multi-level deposition device, wherein said second electrode (112a) is formed over said substantially thin dielectric layer (113), wherein said on-chip capacitor is formed in a crossover area of said first metal layer (111a) and said second metal layer (112a) of said multi-level semiconductor device; wherein said material comprises a composite of materials includes PZT and platinum (see column 10, lines 24-38 and column 12, lines 30-34. Figure 2);

(9) wherein a dielectric constant of said substantially thin dielectric material layer is substantially high due to properties of ferroelectric materials of KNO_3, $PbLa_2O_3$-ZrO_2-TiO_2 (see column 10, lines 24-30. Figure 2);

(12) wherein the second electrode is also deposited on an interface of the second dielectric layer and the second dielectric layer is predetermined to be thicker than the first dielectric layer (see Figure 2).

PRIOR ART REJECTIONS

Statutory Basis

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The Rejections

Claims 10-11 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hirano et al. (U.S. 6,163,043) in view of Tu et al. (U.S. 6,627,493).

Hirano discloses everything above except for applying silicon nitride as material of the first dielectric layer and the thickness of the first dielectric layer. However, Tu discloses a DRAM cell structure with **(10)** wherein said substantially thin dielectric material layer includes silicon nitride (see column 7, lines 50-63); **(11)** wherein said thickness of said substantially thin dielectric material layer is between 50 to 100 Å (see column 8, lines 63-65). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Hirano's device (in accordance with the teaching of Tu) to select specific structure configurations as well as material and thickness of the thin dielectric layer for a capacitor structure, since it has been held that the provision of adjustability, where needed, involves only routine skill in the art. In re Stevens, 101 USPQ 284 (CCPA 1954); In re Aller, 105 USPQP 233.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chuong A. Luu whose telephone number is (571) 272-1902. The examiner can normally be reached on M-F (6:15-2:45).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on (571) 272-1907. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Chuong Anh Luu
Patent Examiner
December 22, 2006